

# Strength in Numbers:

## Core Flight System in a Real-Time Environment on a Multi-Core Space Processor

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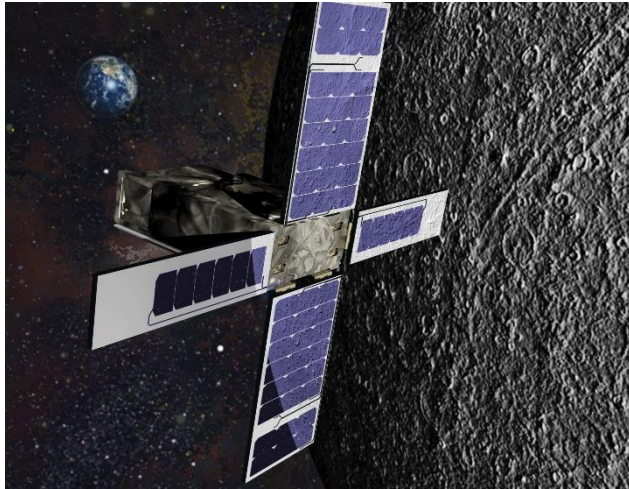


# Agenda

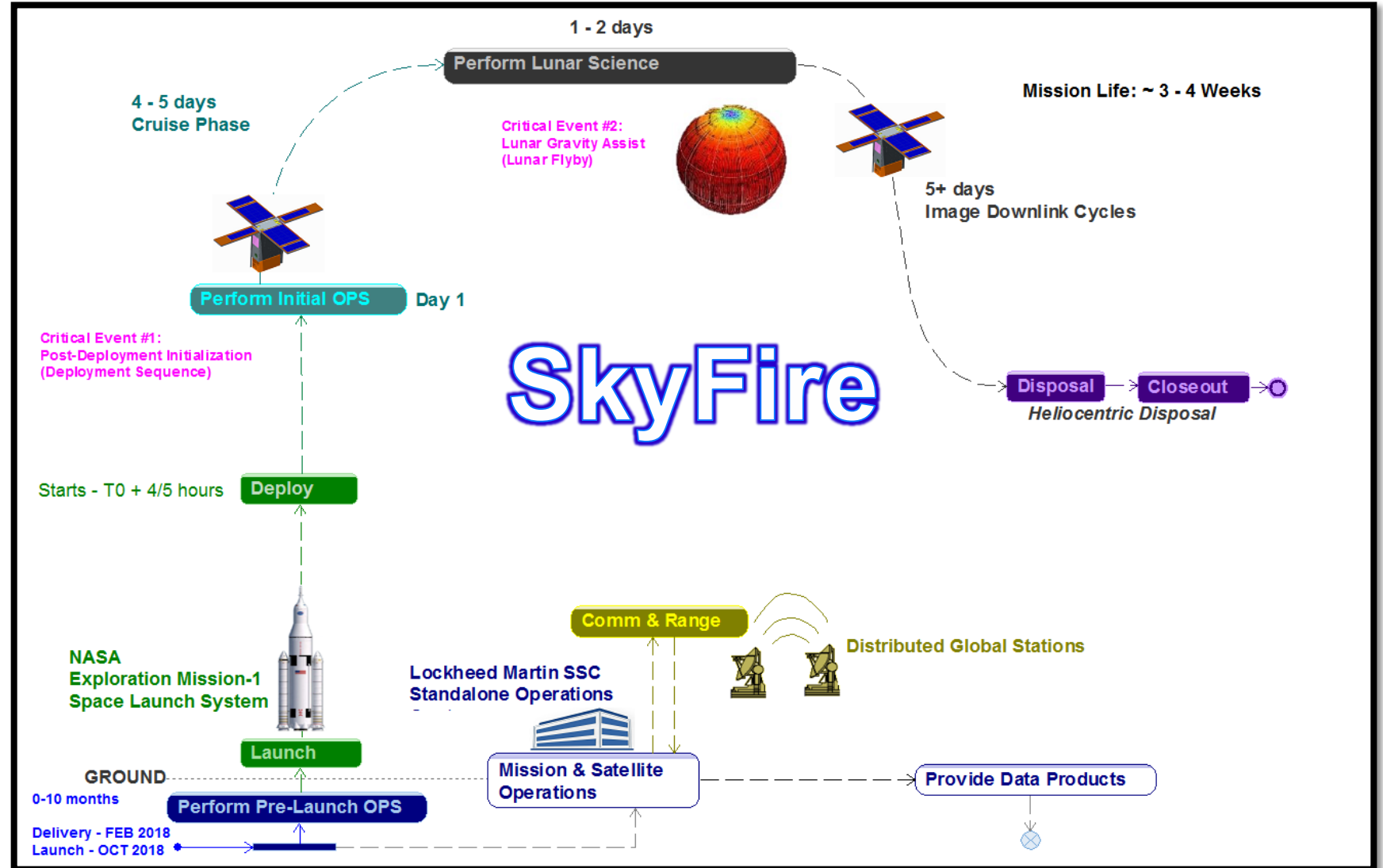


- **Motivation**
- **SkyFire Flight Software**
- **CHREC Space Processor**
- **RTEMS Board Support Package**
- **Operating System Abstraction Layer**
- **Platform Support Package**
- **Successes and Challenges**
- **Future Work**

# Motivation



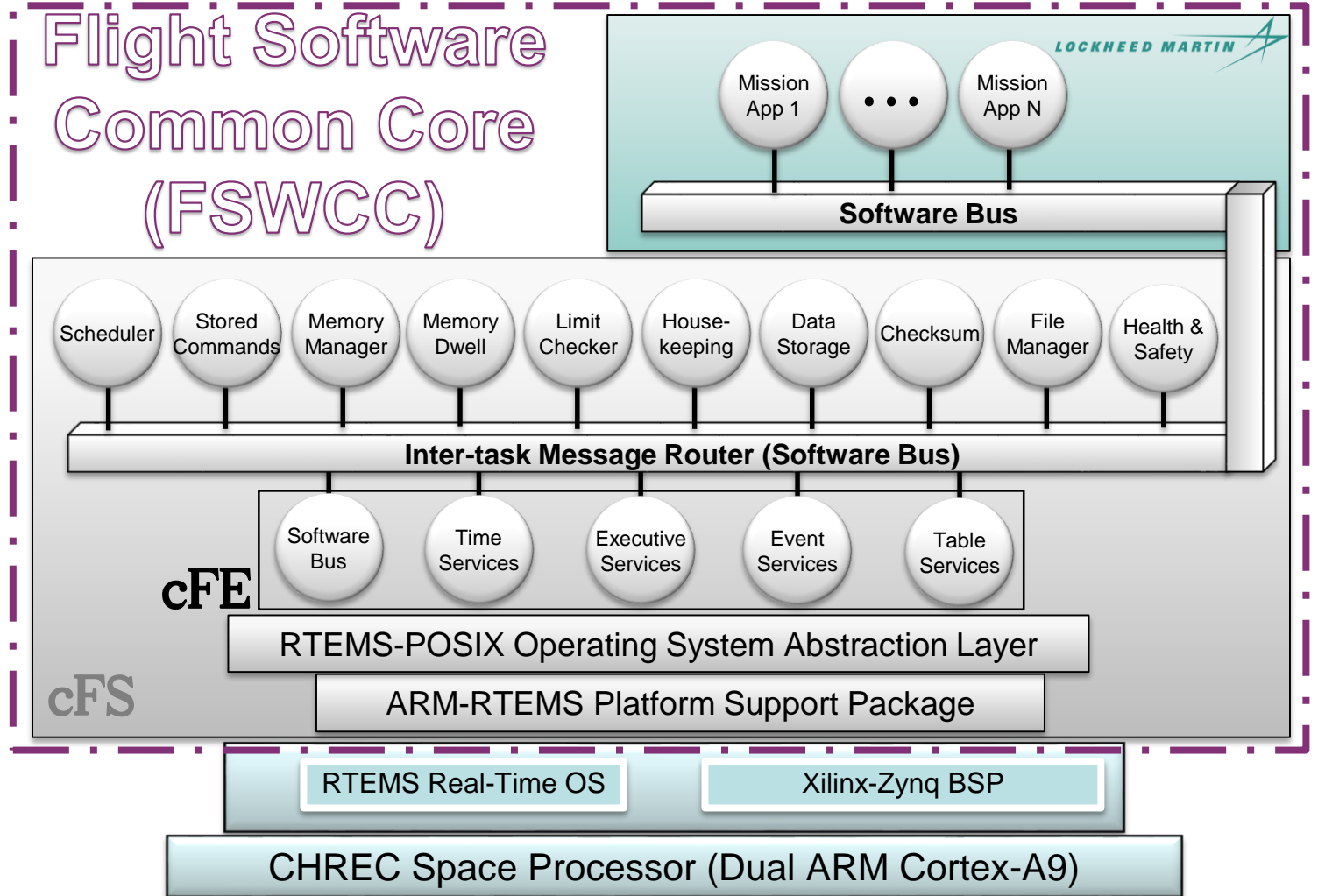
- NASA NextSTEP Cube Satellite
- 6U Form Factor
- Lunar Flyby Mission
- Demonstration platform
- NASA cFS
- CHREC Space Processor



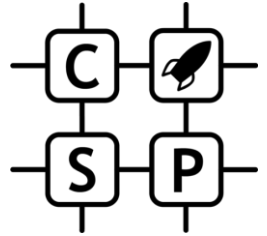
# SkyFire Flight Software Baseline



- 2015**
- Nov. — Baselined FSWCC & CHREC Space Processor (CSP)
- Feb. — Baselined RTEMS 4.11
- May — Demonstrated FSWCC on RTEMS/Zedboard
- Jun. — Upgraded to cFS 6.5
- Jul. — Demonstrated FSWCC on RTEMS/CSP
- 2016**



# CHREC Space Processor v1



- **Motivation**

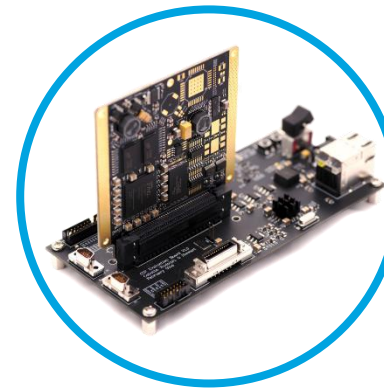
- Create a scalable, high performance, lower power, reconfigurable, and high reliability development system to meet future mission needs

- **Overview**

- CHREC Space Processor v1 (**CSPv1**) is first design in family of CHREC-developed boards embodying CSP concept
- Unique selective population scheme supports assembly of Engineering Model (EM) or flight design
- Flexible app speedup with hybrid and reconfigurable architecture coupled with cost-effective prototyping

- **Keystone Principle**

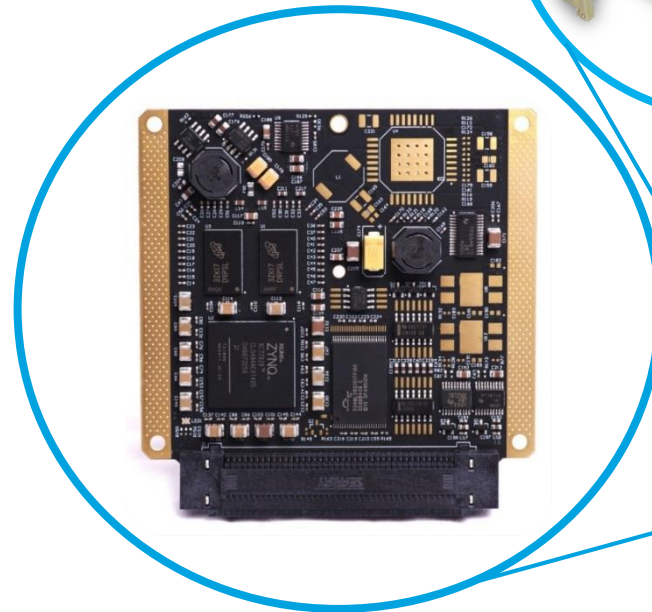
- Commercial technology featured, for best in high performance and energy efficiency, but monitored by radiation-hardened devices, and augmented with fault-tolerant computing strategies



Evaluation Board



Example Flight Configuration



(CSPv1)  
CHREC  
Space Processor

# RTEMS Real-Time Operating System



- **Xilinx Zynq supported in RTEMS**
  - ZedBoard and QEMU Board Support Packages available
  - CSP uses NAND rather than SD non-volatile memory
- **ARM PrimeCell PL350 series NAND controller driver developed**
- **SPI driver for Zynq processing system developed**
- **Future Plans**
  - Xilinx Zynq Device Configuration (DevCfg) driver
    - Allows FPGA reconfiguration and scrubbing at runtime
  - Submit device driver and BSP patches to RTEMS upstream



# cFS Operating System Abstraction Layer Porting

- **Started with POSIX OSAL**
  - Primary benefit: POSIX libdl for runtime loading, rather than CEXP
    - CEXP has no ARM support
- **Challenges**
  - ARM cache problems after application load (now patched in upstream RTEMS)
  - RTEMS ARM Run Time Loader (RTL) object cache bug
  - RTEMS ARM RTL unable to handle weak symbols bug
  - RTEMS is *mostly* POSIX compliant
    - *SA\_RESTART* flag unsupported
    - *dlderror* non-conformance
  - cFS OSAL initialization thread priority
    - Complications from applications preempting the init thread



# cFS Platform Support Package Porting

- **Ported *pc-linux* PSP**
- **Minimal modification due to POSIX compliance**
- **RTEMS timer server used for cFE 1 Hz timer**
  - Tick function requires thread context
- **Challenges**
  - Tricky to resolve undefined symbols from cFE applications in the base image
  - Current workaround is to use 'nm' to list undefined symbols, then force them into the base image





# Successes & Challenges

- **Successes**

- SkyFire flight software is executing on RTEMS/CSP
- Upgrade to cFS 6.5 was virtually seamless
- RTEMS issues patched/fixed
  - Thank you to RTEMS mailing lists/Chris Johns/Pavel Pisa/Joel Sherrill
- cFS OSAL & PSP were great starting points for port to ARM-RTEMS

- **Challenges**

- Pathfinders for RTEMS ARM runtime loader
- Porting *pc-linux* OSAL to *arm-rtems*



# Future Work

- **Lockheed Martin SkyFire**
  - Integrate final revision of CSP NAND Flash
  - Software-hardware integration
  - Functional verification testing
  - Deliver March 2018
- **CHREC**
  - Continue increasing RTEMS support for CSPv1
  - Expansion to University of Pittsburgh

