RAD55xx Platform SoC

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*** photo courtesy of NASA
Agenda

- RAD55xx Platform SoC Introduction
- Processor Core / RAD750® Processor Heritage
- SoC Personalities and Peripheral Logic
- RAD5545™ SBC
- A Glimpse at SpaceVPX and Serial RapidIO
- Software Considerations in Deploying RAD55xx Systems
One RAD55xx Platform System-on-Chip (SoC) Replaces:

- Four RAD750® microprocessors
- Four L2 cache MCMs
- Enhanced Power PCI bridge ASSP
- Rad-hard NAND Flash controller FPGA
- Four 4-port SpaceWire router ASSPs
- Rad-hard dual interleaved DDRx DRAM controller ASSP
- Two rad-hard FPGAs with RapidIO cores and SerDes I/O
- Four rad-hard AES encryption ASSPs
- Rad-hard digital signal processor bridge application specific standard product (ASSP) or FPGA
- Rad-hard FPGA with Ethernet core including partial TCP/IP offload, IEEE 1588 timing function, and SerDes I/O

A single RAD55xx platform SoC integrates many ASSP/FPGA processors and peripherals, with a massive improvement in power/performance vs. current production technologies.
One Platform Die: Multiple Personalities

RAD5510™ microprocessor: enhanced SoC follow-on to the RAD750® microprocessor

RAD5515™ microprocessor: single core SoC with RapidIO serial links

RAD5545™ microprocessor: Quad core high performance processor SoC

The RAD55xx platform SoC can be personalized into many different processors with unique features and power/performance characteristics.
The RAD5500 core is BAE System’s 3rd generation Rad-hard Power Architecture processor.
Processor Core and Peripheral Logic Documentation

- **RAD6000® processor**
  - POWER Processor Architecture Version 1.52
- **RAD750® processor**
  - PowerPC™ Microprocessor Family: The Programming Environments For 32-Bit Microprocessors
  - PowerPC 750™ RISC Microprocessor User’s Manual
  - BAE Peripheral Logic:
    - Golden Gate Bridge (now called RADNET™ SpW-RB4) Programmer’s Reference Manual
- **RAD5500™ processor family**
  - EREF 2.0: A Programmer’s Reference Manual for NXP/Freescale Power Architecture® Processors
  - e5500 Core Reference Manual
  - Platform SoC:
    - RAD5545 SoC Processor Product Brief
    - RAD55xx QorIQ® Integrated Multicore Processor Reference Manual
      - Significant overlap w/ P5020 QorIQ Integrated Multicore Processor Reference Manual
    - RAD55xx Stonewall Complex Reference Manual
      - Significant overlap w/ Golden Gate Bridge Programmer’s Reference Manual
    - QorIQ Data Path Acceleration Architecture (DPAA) Reference Manual
      + Addendum for RAD55xx

**Processor core compatibility with commercial design enables use of 3rd party software**

QorIQ is a trademark of NXP semiconductors
The RAD55xx platform SoC can be personalized to meet application needs.
The RAD5500™ Microprocessor Core

64/32-bit Power Architecture®

- Features:
  - Superscalar dual-decode, quad-issue: out-of-order execution/in-order completion
  - IEEE 754 double-precision floating point unit
  - 512 KB backside L2 cache with Tag and Data ECC
  - 32 KB Instruction & Data L1 caches with Tag and Data ECC and write shadow mode
  - ‘Book E’ MMU w/ Large L2 translation lookaside buffers (TLB)
  - 36-bit physical address, 64-bit virtual address
  - Improved branch prediction
  - New instructions for byte and bit-level acceleration
  - Real-time trace / debug interface

- Enhancements for multicore operation
  - Improved snoop capabilities
  - Inter-core messaging support
  - Full cache MESI coherency, intervention, locking, and stashing
  - Embedded Hypervisor

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The 64-bit RAD5500 core is 32-bit compatible with improved performance and reliability

<table>
<thead>
<tr>
<th>Core comparison</th>
<th>RAD750 core</th>
<th>RAD5500 core</th>
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<tr>
<td>Dhrystone</td>
<td>2.2 MIPS/MHz</td>
<td>3 MIPS/MHz</td>
</tr>
<tr>
<td>Double precision FPU</td>
<td>1 OP/cycle</td>
<td>2 OP/cycle</td>
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<td>General purpose regs</td>
<td>32-bit</td>
<td>64-bit</td>
</tr>
<tr>
<td>Integer units</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Cache line size</td>
<td>32 bytes</td>
<td>64 bytes</td>
</tr>
<tr>
<td>ECC on arrays</td>
<td>none</td>
<td>All arrays</td>
</tr>
<tr>
<td>Physical Addressing</td>
<td>4G</td>
<td>64G</td>
</tr>
</tbody>
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RAD55xx Platform SoC Data Path Acceleration Architecture

RAD55xx SoC DPAA components

- **Infrastructure**
  - Queue Manager (QMAN):
    - Prioritized queuing of descriptors
    - Shared queues for load spreading
    - WRED* active queue management
    - Pre-positioning of data into core cache
  - Buffer Manager (BMAN):
    - 64 pools of buffer pointers
    - Acquisition/release of pointers to/from pools

- **Network I/O**
  - Ethernet Frame Manager (FMAN):
    - Partial L2, L3, L4 protocol offload
    - IEEE 1588 time stamping
  - Four RapidIO Message Managers (RMAN):
    - Message and streaming packet types
    - Segmentation/reassembly of multiple segment packets

- **Hardware accelerator**
  - SEC – cryptographic accelerator
    - Cryptographic authentication
    - Public key and encryption algorithms
    - Run time integrity checking

- **RAD5500™ processor cores**

For more information: Freescale DPAA reference manual

DPAA utilizes infrastructure and accelerator components to free up the processor cores.

*WRED = weighted random early detection
RAD55xx Platform “Trust Architecture” Elements

- **Multi-phase Secure Boot**
  - Initial boot process stored on-chip ROM can validate external boot code via RSA public key cypher prior to execution

- **Processor cores** support User, Supervisor and Guest states
  - Memory address translation look-aside buffers contain bits to control whether memory pages can hold User mode or Supervisor mode executable code
  - Embedded hypervisor architecture allows hypervisor software to run at the most privileged level to control virtualization of the RAD55xx SoC and prevent critical settings from being modified by the operating system or application software

- **Memory access control** is enforced for processor cores and DMA engines
  - Memory management units enforce access control for processor cores
  - Peripheral access management units (PAMU) control non-processor core access to memory regions unless access is explicitly granted

- **Memory integrity** can be automatically checked using cryptographic hashing

- **Security Engine (SEC)** supports multiple block ciphers, public key cryptography, cryptographic authentication and random number generation

- **Security Monitor** provides real-time security state sensing and control

- **Secure debug controller** with four levels of access supports lab and field debug modes and fully blocked mode while still allowing JTAG boundary scan

Trust architecture combined with appropriate software provides a more secure boot and operating environment with fault detection capabilities.
RAD5545™ 32/64-bit System-on-Chip Multi-Core Processor

- Four RAD5500™ cores
  - 5.6 Dhrystone GIPS / 3.7 GFLOPS
  - Fully compatible with 32-bit software
- CoreNet™ coherency fabric with Data Path Acceleration Architecture
- Hardware assisted processor pooling, load leveling, and buffer management
- Peripheral access management unit (PAMU) controls external device access to memory space
- Encryption hardware accelerator
- **Dual interleaved** DDR2 / 3 DRAM interfaces @ 800 MT/s
- Four “x4” RapidIO ports provide up to 64 Gbps I/O throughput
- SerDes-based real time trace/debug
- SRAM / C-RAM interfaces
- NAND Flash controller
- **Sixteen port** SpaceWire router
- **32-bit PCI parallel bus**
- 27 DMIPS Embedded Microcontroller (EMC)

The RAD5545 SoC balances multiple Power Architecture™ cores with DDR DRAM and Gigabit serial links to maintain peak performance across a variety of applications.
Outfitted with high performance DDR3 memory and TMR protected flash memory, RAD5545 SBC is personalized for various applications using a daughter card.
RAD5545 SBC Module Features

- Card format: 6U-220 SpaceVPX (payload and/or controller profile)

- RAD5545 quad-core system-on-chip processor platform ASIC
  - Card can be personalized as RAD5515™ SoC, or RAD5510™ SoC with minimal modifications

- Compatible with highest availability RAD® DDR3 REM DIMM or high reliability RAD® DDR3 DIMM or COTS XR-DIMM DDR3 memory modules
  - 2-16 GB of error corrected DDR3 SDRAM

- Up to 8 GB of TMR NAND flash

- One utility FPGA
  - Control/voter for triplicated NAND flash
  - SpaceVPX controller interface signals
  - Pulse per second timing signal
  - Power sequencing
  - Parallel bus interface to RAD5545 SoC

- Backplane interfaces
  - 3 (optionally 4) x4 RapidIO interfaces to the SpaceVPX backplane @ 5 Gbaud/lane
  - Up to two Gbit Ethernet interfaces to the backplane
  - 12 SpaceWire ports to the backplane

- Mezzanine daughter card for I/O or logic customization, such as MIL-STD-1553B fed by:
  - Four SpaceWire ports
  - 32-bit PCI
  - I2C
  - Optionally one x4 RapidIO interface (mutually exclusive with 4th backplane interface)
  - Module derived POL power

  Power is dependent on frequency, function and interface usage.
SpaceVPX: A Glimpse

- VITA 78 defines SpaceVPX, building on existing VITA / VPX standards
  - Extends Utility Plane for fault tolerance
  - Defines use of SpaceWire for Control Plane
- Defines Payload, Switch, Controller, and Backplane module profiles
RapidIO: A Glimpse

- Packet switched interconnect
  - Packet acknowledge/retry
  - Priority levels
- Serial RapidIO (SRIO) SerDes
  - 8b/10b encoding
  - 1.25, 2.5, 3.125, 5.0, 6.25 Gbaud link rates
  - 1x, 2x, 4x lane links defined in SpaceVPX

- Many logic transaction types:
  - MAINTENANCE for system config, discovery, etc.
  - NREAD, NWRITE, NWRITE_R, SWRITE perform remote memory access
  - MESSAGE for network message passing
  - DOORBELL short message (e.g., interrupts)
  - Data Streaming for lossy high rate streaming
Software Architecture Considerations

- Application memory model: 32-bit, 64-bit, or mixed applications
  - Options depend on OS and tools
  - Potential problems running legacy 32-bit code in 64-bit mode
- Operating System(s) selection
- Multi-core considerations:
  - SMP (Symmetric Multiprocessing)
    - Single OS allows CPU resources to easily be shared
    - Don’t expect a full 4x throughput increase on quad-core system
      - Cache misses can limit performance
      - Affinities can help with tuning
    - Potential problems with legacy code critical sections
      - OS semaphores, mutexes, etc. are SMP-safe
  - Embedded Hypervisor
    - Allows multiple guest OSes
    - OS/Hypervisor compatibility
  - AMP (Asymmetric Multiprocessing)
    - Limited flexibility
- Application address space partitioning: user-space vs. kernel-space
- Application time partitioning
- Define key SoC peripheral functions: SRIO, SpaceWire, security, encryption, etc.
Thank You

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