Updates on the Software Development Environment for the new GR716 LEON3FT Microcontroller

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This presentation does not contain any ITAR information

Overview

- GR716 microcontroller hardware
  - With a software perspective
- Upcoming TSIM3 and TSIM-GR716 BETA
  - LEON system simulator
- BCC2
  - Bare metal toolchain for LEON processors
- GRMON3
  - LEON system hardware debugger and monitor
- GR716 hardware availability

GR716 – LEON3FT Microcontroller

Introduction

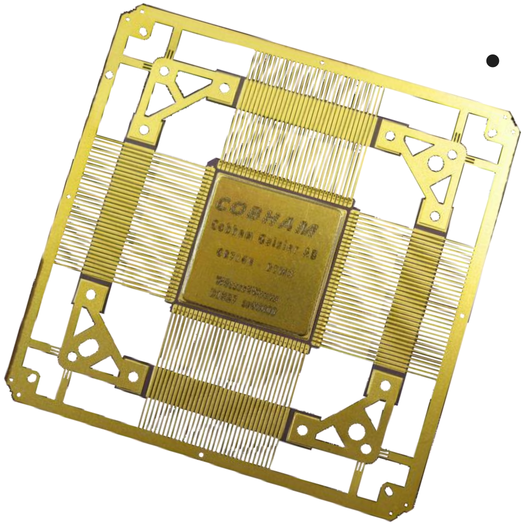
Description

The GR716 features a fault-tolerant LEON3 SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications

Applications

Support for many different standard interfaces makes the GR716 microcontroller is ideally fit for handling supervision and control in a satellite, such as

- propulsion system control
- sensor bus control
- robotics applications control
- simple motor control
- mechanism control
- power control
- particle detector instrumentation
- radiation environment monitoring
- thermal control
- antenna pointing control
- remote terminal unit control
- simple instrument control



Specifications

- System frequency up-to 50 MHz
- SpaceWire links up-to 100 Mbps
- CQFP132 hermetically sealed ceramic package
- Total Ionizing Dose (TID) up to 100 krad (Si, functional)
- Single-Event Latch-Up (SEL) to $\mathrm{LET}_{\mathrm{TH}}$ > 118 MeV-cm^{2}mg
- Single-Event Upset (SEU) below 10^{-12} bit error rate
- Support for single 3.3V supply

esa

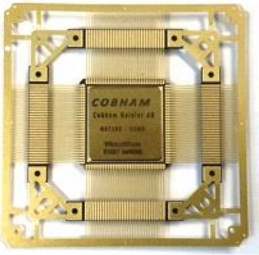
COBHAM
Cobham Gaisler AB

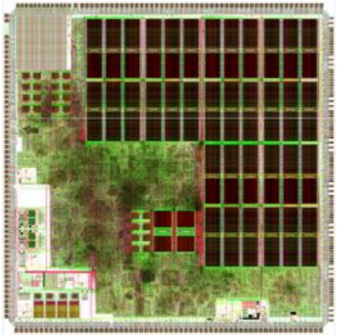
imec

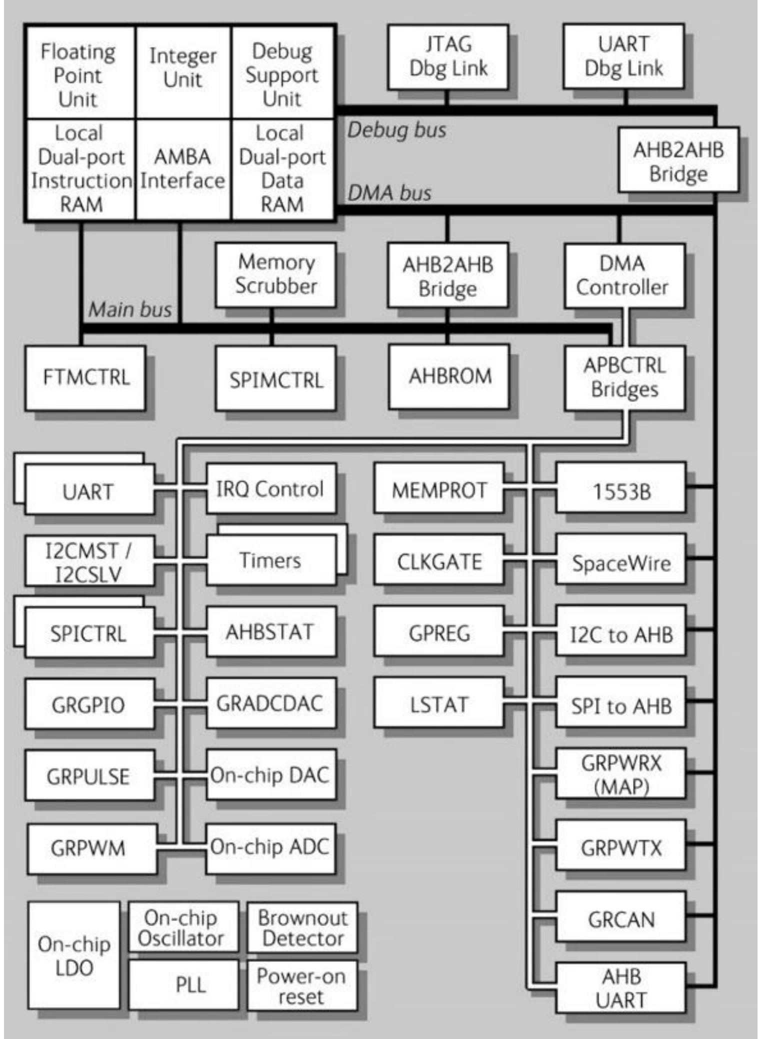
GR716 – LEON3FT Microcontroller

Overview

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - 16-bit instruction set: LEON-REX - improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
- External EDAC memory: 8-bit PROM/SRAM, SPI, I²C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I²C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- DAC 12bits @ 3Msps, 4 channels
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm







GR716 boot ROM

- Boot configuration through pin strapping
- Built in bootloader in ROM
  - Derived from JUICE mission bootloader
- Supports boot from multiple memory sources
  - RAM, PROM, SPI, I^{2}C
- Multiple modes
  - Load ASW images with CRC verification
    - With possibility of a redundant backup
  - Continue execution in chosen memory
  - Remote mode where external entity loads application
- Mkprom not needed
- ROM Bootloader can also be bypassed
  - Executing directly from RAM, PROM or SPI

HW features benefitting flight software

- 192KiB tightly coupled memory, local RAM
  - 128 KiB for instructions and 64KiB for data
  - ideal for hard real-time embedded control applications in space environments requiring a high level of determinism
  - Available also from the bus for DMA
  - No timing interference between CPU and DMA
- Atomic operation support
  - And, Or, Xor, and Set & clear
  - For local memory
  - For I/O core registers
  - Both for CPU and DMA

HW features benefitting flight software

- Partial PSR write
  - Enabling and disabling traps atomically
  - More efficient PSR updates
- 31 register windows
  - Can reduce or alleviate need for register window traps
  - Window space can be partitioned for different uses
- Interrupt mapping
  - Allows user determined interrupt prioritization
- IRQ timestamping and CPU-local time source
  - Allows for precise timing when handling interrupts
- A new compact instruction set reducing memory footprint

LEON-REX

New compact instruction set

- Thin layer that translates LEON-REX instructions to standard SPARC instructions during execution
  - Available after entering REX mode
  - No change to register widths or calculation results
- Main addition is 16-bit versions of common instructions
  - Only two registers and no immediates for most instructions
  - Can only access half of available registers
  - add %i0, %i2, %i0 <-> radd %i2, %i0
    [0xb0, 0x06, 0x00, 0x1a] [0xa0, 0x0a]
- Most 32-bit instructions still available (including floating point)
  - Exceptions are: UNIMP and SETHI
  - Can access all available registers
  - Immediate field only 7 bits instead of 13
- 48-bit instructions handling 32 bit constants or addresses

LEON-REX

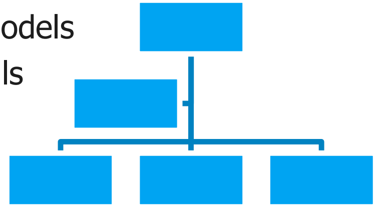
New compact instruction set

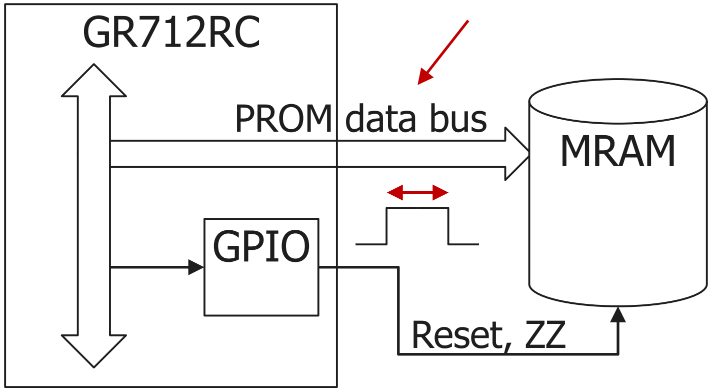
- Compatible with SPARC ABI
  - REX compiled code can be used together with standard SPARC compiled code
- Enter REX mode in function prologue with SAVEREX or ADDREX
  - save %sp, -96, %sp -> saverex %sp, -96, %sp
  - add %sp, -80, %sp -> addrex %sp, -80, %sp
- Function calls and traps enters standard SPARC mode
- Least significant bit in PC signifies REX mode
  - Unused since instructions are 16-bit aligned
  - Returning from function reenables REX mode or SPARC mode depending on return address
- Developed by Cobham Gaisler
- Details available in technical note at Cobham Gaisler webpage

TSIM

ERC32 and LEON system simulator

- Simulator for ERC32 and LEON2/3/4 systems
  - Instruction-level simulation
  - High level of accuracy
  - Highly extensible
- Standard simulator for LEON (over 500 sold licenses)
- Multiple modes of operation
  - Standalone operation
  - Library interface
  - Remote GNU debugger connection (C/C++ source debug)
- User extensible
  - IO bus and AMBA bus device models
  - Models for connected peripherals
  - FPU and coprocessor models
  - Custom instructions
  - Interrupt controllers
- Integrable into larger simulation frameworks
- Non-intrusive execution statistics
  - General statistics: instructions, caches, bus use
  - Execution profiling
  - Code, decision and data coverage monitoring





TSIM SW validation example:
MRAM 100us power-down time-out, check
GPIO timing and PROM access

TSIM as an interactive debugging tool:

- Breakpoints
- Watchpoints
- Instruction traces
- Stack back traces with symbolic information
- Check-pointing capability to save and restore simulator state
- I/O core event tracing
- RTEMS thread support
- Source level debugging using remote GDB connection

TSIM3 development

TSIM2 and GRSIM successor

- Multiprocessor support
- Support for additional systems
  - GR716
  - GR740
- Support for general system configurations
- New internal architecture to handle more diverse system architectures
- Tcl scripting support
- Support for additional I/O cores
- User extension possibilities for custom models
- Continuing the accuracy profile of TSIM2

TSIM3 and GR716

- Already used internally on a daily basis
  - For testing, debugging and development
- Supports multiple ways of loading applications
  - Load and run directly from local memory or external SRAM
  - Boot using all boot configurations apart from I²C
    - No model for I²C yet
- Many GR716 models in place
  - CPU, FPU, Interrupt controller
    - CPU features new to the GR716
    - Interrupt timestamping and remapping
  - Local RAM that is also accessible from the bus
  - Memory controllers, status registers
  - UARTs, timers, SpaceWire, SPI, GPIO
  - Atomic operations on local RAM and register areas

TSIM-GR716 BETA

- TSIM-GR716 BETA to be released in 2019 Q1

- Will be in between TSIM2 and the upcoming TSIM3
  - GR716 does not need all new features of TSIM3
- Aforementioned GR716 support
- Tcl scripting support
- Improved debugging features
- User model APIs available for extensions
  - Albeit not in final TSIM3 form

- Some limitations for existing TSIM2 features
  - They will be available again in TSIM3

BCC2

- Bare metal toolchain for LEON processors
  - C/C++ cross compilers, both GCC and LLVM/Clang
  - C/C++ standard libraries
  - Open source with permissive licenses
- Support for GR716
  - Basic support for the GR716 architecture
    - Memory map, interrupts, capabilities
    - Linker scripts
    - ROM resident images
  - Support for GR716 features
    - REX
    - Single Vector Traps
    - Can generate chip specific instructions
  - Device drivers for GR716 I/O cores
  - Flat mode – staying in one register window
    - Can reduce jitter
    - Can be used with register window partitioning
  - Optional C runtime with even smaller footprint
    - Newlib nano

Adjusting to different profiles

Property	Performance	Footprint	IRQ Response time
More register windows	+	~	~
Optimize for size	-	+	~
Single Vector Trapping	-	+	-
Newlib nano C runtime		+	~
REX	-	+	
Flat mode	*	-	+
Soft mul/div	-	-	+
Soft float	-	-	+
IRQ jitter reduction	-	~	-

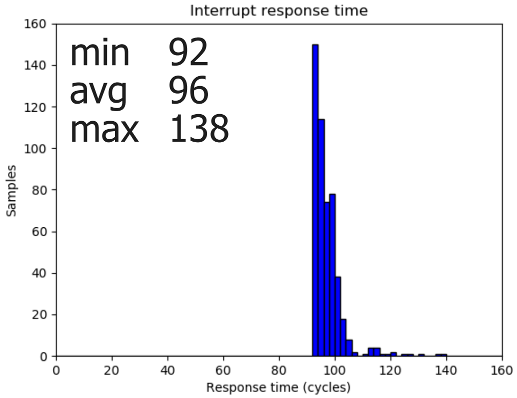
Effects in general for the given metric:

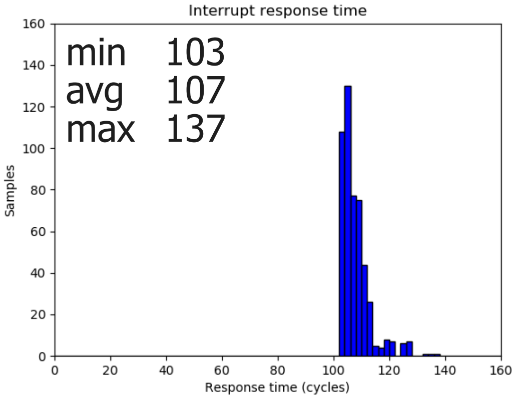
+	better	*	Varies
-	worse		
~	marginal		

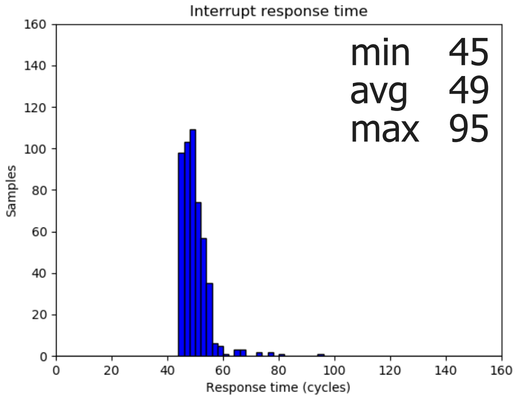
Example of different profiles

Whetstone

Performance mode	Footprint mode	Response time mode
6.9 s execution time	11.5 s execution time	7.0 s execution time
130 KiB footprint	76 KiB footprint	138 KiB footprint







Adding soft mul/div/float takes down max IRQ repose time to 52 cycles in this example, but at the cost of an execution time of 248 s

- Needed stack space not included in footprint numbers

- Effects are application specific
- Options can be mixed and matched to suit the application

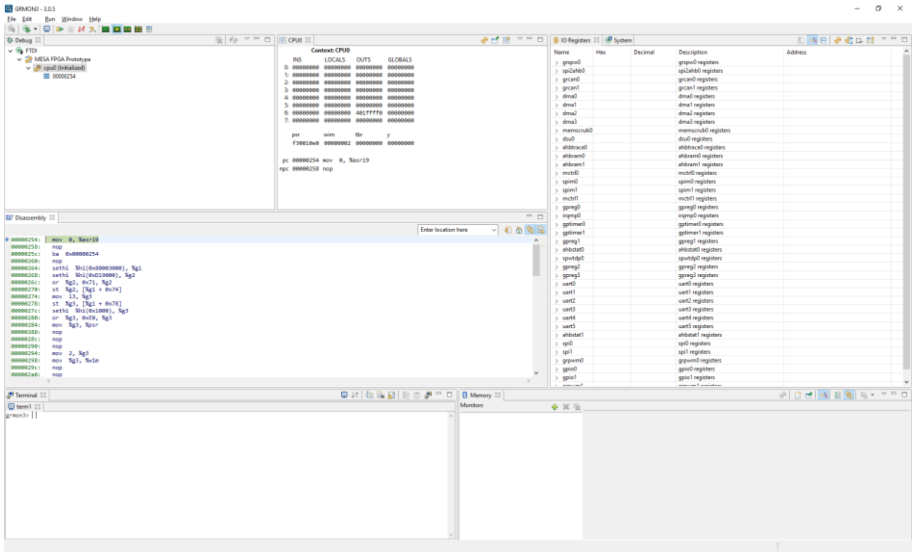
GRMON 3

Features

- Hardware debugger and monitor for LEON systems
- Has both a CLI and a GUI
- Read/write access to all LEON registers and memory
- Execution control with support for multiple CPUs and OS threads
- Built-in disassembler and trace buffer management
- Breakpoint and watchpoint management
- Remote connection to GNU debugger (GDB)
- Auto-probing and initialization of LEON peripherals and memory settings
- Error injection for fault-tolerant LEON processors
- Supported debug interfaces: USB, Ethernet, JTAG, UART and SpaceWire
- Common Flash Interface (CFI) compatible Flash PROM programming
- TCL scripting support
- In-application help for all commands
- Context-based virtual memory handling
- Translates virtual addresses for GDB, e.g. it's possible to debug the VxWorks/Linux kernel

Specific GR716 support in GRMON3

- Register support for all IP cores
- Alternative Window Pointer support
- Clockgating support
- REX support
  - Disassembly
  - Backtraces
  - Instruction trace
    - executed SPARC v8 instructions
  - Breakpoints



```
          Context: CPU0

    INS       LOCALS    OUTS      GLOBALS
 0: 00000000  00000000  00000000  00000000
 1: 00000000  00000000  00000000  00000000
 2: 00000000  00000000  00000000  00000000
 3: 00000000  00000000  00000000  00000000
 4: 00000000  00000000  00000000  00000000
 5: 00000000  00000000  00000000  00000000
 6: 00000000  00000000  401ffff0  00000000
 7: 00000000  00000000  00000000  00000000

    psr       wim       tbr       y
    f30010e0  00000002  00000000  00000000

 pc 00000254 mov  0, %asr19
npc 00000258 nop
```

```
00000254:  mov  0, %asr19
00000258:  nop
0000025c:  ba  0x00000254
00000260:  nop
00000264:  sethi  %hi(0x80003000), %g1
00000268:  sethi  %hi(0xD19000), %g2
0000026c:  or  %g2, 0x71, %g2
00000270:  st  %g2, [%g1 + 0x74]
00000274:  mov  13, %g3
00000278:  st  %g3, [%g1 + 0x78]
0000027c:  sethi  %hi(0x1000), %g3
00000280:  or  %g3, 0xE0, %g3
00000284:  mov  %g3, %psr
00000288:  nop
0000028c:  nop
00000290:  nop
00000294:  mov  2, %g3
00000298:  mov  %g3, %wim
0000029c:  nop
000002a0:  nop
```

```
grmon3> |
```

Name	Hex	Decimal	Description	Address
grspw0			grspw0 registers	
spi2ahb0			spi2ahb0 registers	
grcan0			grcan0 registers	
grcan1			grcan1 registers	
dma0			dma0 registers	
dma1			dma1 registers	
dma2			dma2 registers	
dma3			dma3 registers	
memscrub0			memscrub0 registers	
dsu0			dsu0 registers	
ahbtrace0			ahbtrace0 registers	
ahbram0			ahbram0 registers	
ahbram1			ahbram1 registers	
mctrl0			mctrl0 registers	
spim0			spim0 registers	
spim1			spim1 registers	
mctrl1			mctrl1 registers	
gpreg0			gpreg0 registers	
irqmp0			irqmp0 registers	
gptimer0			gptimer0 registers	
gptimer1			gptimer1 registers	
gpreg1			gpreg1 registers	
ahbstat0			ahbstat0 registers	
spwtdp0			spwtdp0 registers	
gpreg2			gpreg2 registers	
gpreg3			gpreg3 registers	
uart0			uart0 registers	
uart1			uart1 registers	
uart2			uart2 registers	
uart3			uart3 registers	
uart4			uart4 registers	
uart5			uart5 registers	
ahbstat1			ahbstat1 registers	
spi0			spi0 registers	
spi1			spi1 registers	
grpwm0			grpwm0 registers	
gpio0			gpio0 registers	
gpio1			gpio1 registers	

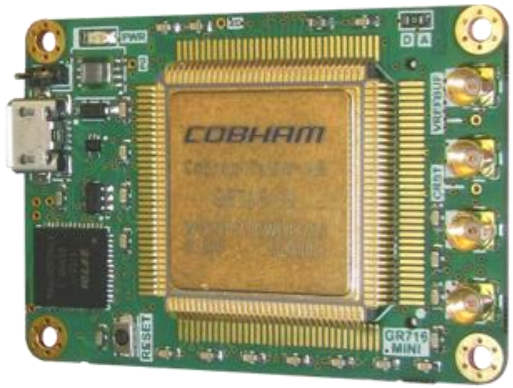
GR716 Roadmap

- Releases planned for 2019 Q1
  - GR716 prototypes available
  - TSIM-GR716 BETA
  - Extended GR716 driver support for BCC
  - Application notes
- TSIM support for GR716 will be part of TSIM3
  - Support for GR716 architecture
  - Built in support for major I/O cores
  - User extendable for other I/O cores
- BCC and TSIM support for major I/O cores planned
  - SpaceWire
  - CAN
  - MIL-STD-1553B
- Evaluation of Zephyr RTOS for GR716

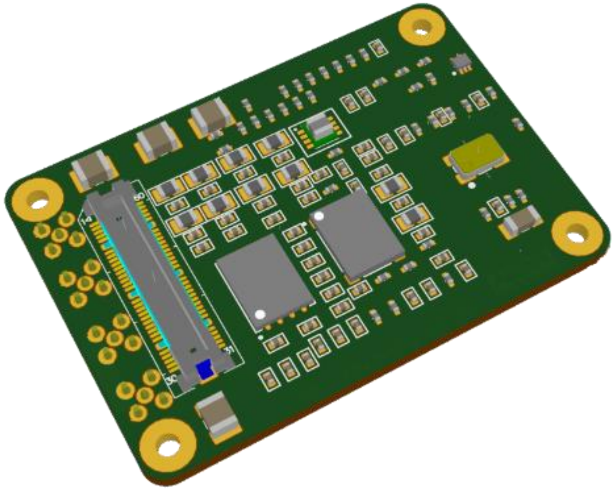
GR716 evaluation board

GR716-MINI – GR716 Software evaluation board

- Baseline design for evaluation board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - SRAM (2 MiB)
  - FTDI USB interface
    - GRMON3 debug I/F via Debug UART
    - 2x UART interfaces, 1x I^{2}C interface
    - control of reset, configuration pins etc.
    - power supply
  - 4x MMCX (micro-miniature coaxial):
    - 2x ADC, 2x DAC
  - miniature 80 pin mezzanine connector:
    - addition ADC, DAC, LVDS, GPIO, etc.
  - Oscillator
  - LED for power indication etc.
  - 50mm x 35mm (37.5% of a credit card)



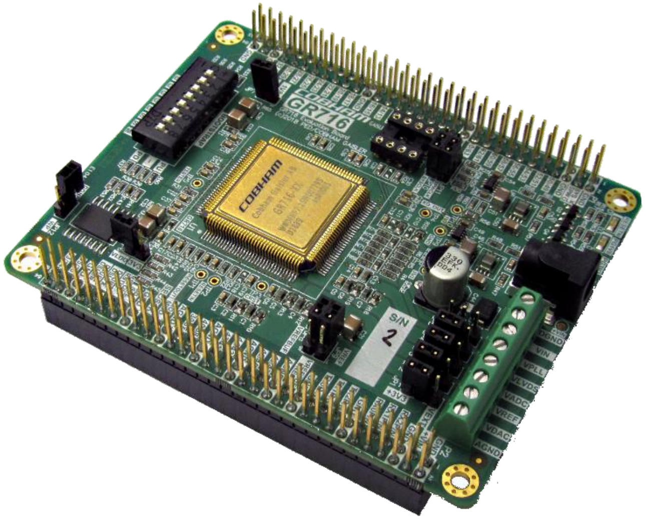
- Shipped with:
  - free GRMON3 GUI (limited) download
  - free compilers, OS, tools downloads
  - USB cable (debug and power)



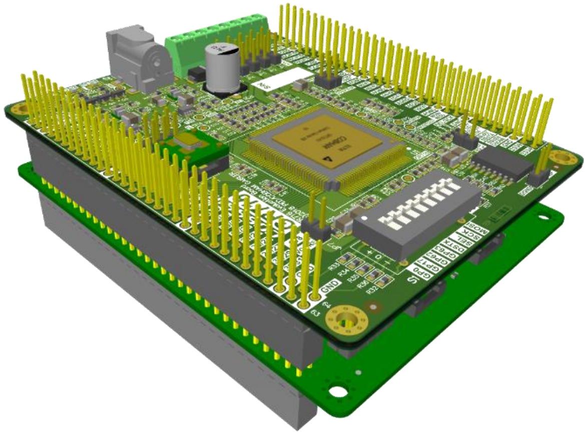
GR716 development board

GR716-BOARD – GR716 Hardware engineering board

- Baseline design for development board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - PCI104 style stackable headers (2 x 64 pin) for interfaces
    - measurement points on all GPIO/interface signals for monitoring/debug
    - interface to user defined modules (memory, digital I/F, analog I/F)
    - interface to cPCI mother board in 6U rack or box format
  - Debug UART /IF
  - LVDS in/out (3+3 pairs) for 1x SpW or x SPI for Space
  - GPIO (64 pins)
    - digital I/O
    - external memory I/F
    - 6x UART
    - Mil-Std-1553B, PacketWire, CAN, I^{2}C, 3x SPI, 16x PWM out
    - 8x analog in, 4x analog out, external ADC/ADC interface
    - 1x SpaceWire, 1x TDP
  - Socketed oscillator (5–25MHz)
  - DIP-switch for bootstrap options
  - Powered from external supply (range 5V to 12V)
  - Single supply operation or individual supplies
  - 80mm x 100mm format



GR716 Standalone Board

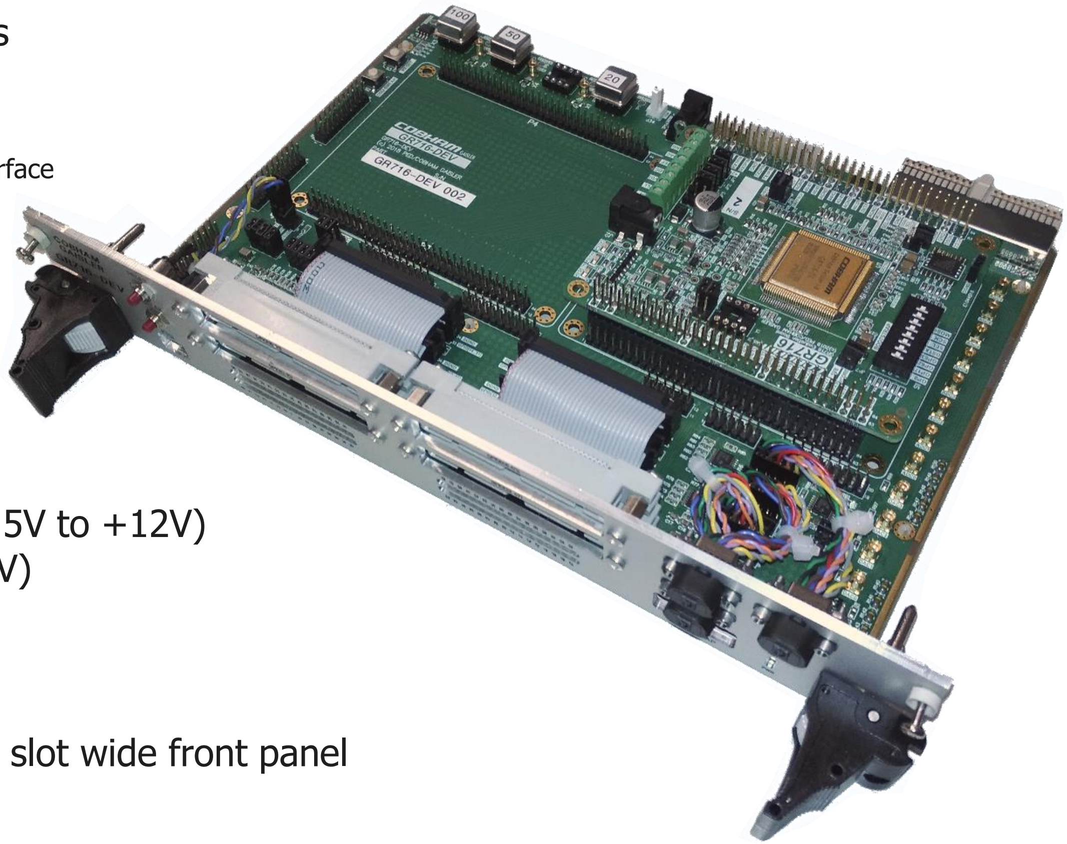


Stack multiple boards via PC104 connector

GR716 development board

GR-CPCI-GR716-DEV – GR716 interface development board

- Baseline design for interface application board:
  - GR716-BOARD engineering board in dedicated slot
    - Multiple slots for possibility to attach multiple GR716 engineering boards
  - Expansion slot for memory or user defined functions (e.g. SRAM, ADC/DAC)
  - Socketed oscillators for system, SpaceWire, Mil-Std-1553B and PWM clocks
  - Configuration of front panel functions
  - Front panel interfaces
    - MDM9S for fixed SpW (LVDS) interface
    - MDM9S for configurable SpW/SPI4S (LVDS) interface
    - GPIO (64 pins on standard 0.1" connectors)
    - LED indicators (64) for GPIO pins
    - DIP switch for bootstrap options
    - Reset and DSU Break push-button switches
    - LEDs for power and reset status
    - FTDI USB interface
      - GRMON3 debug I/F via Debug UART
      - 2x UART interfaces, 1x I^{2}C interface
  - Power from external supply (range +5V to +12V) or via cPCI backplane connector (+5V)
  - Expansion through accessory boards
    - 6x UARTs using GR-CPCI-6U-UART
    - CAN, Mil-Std-1553B, SPI using GR-CPCI-GR740
  - 233mm x 160mm, 6U cPCI format, 2 slot wide front panel



Thank you for listening

TSIM

SPARC

GRMON3 debugging made easy