MultiChipSat: an Innovative Spacecraft Bus Architecture

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Outline

- Motivation
- Objectives
- Architecture Overview
- Other architectures
- Hardware architecture
- Software architecture
- Challenges

Introduction

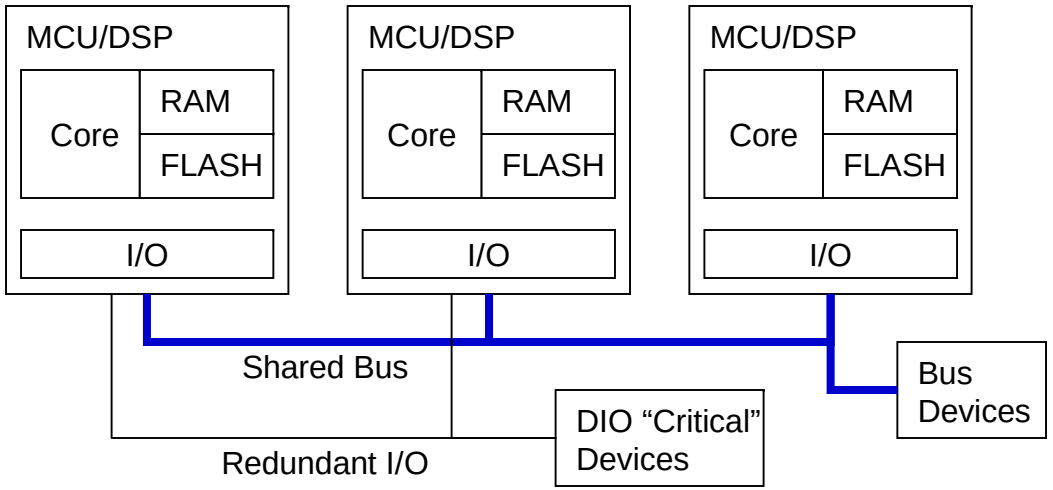
- Can distinguish two trends in microprocessor requirements:
  - Require high processing power for new complex missions, developed using COTS CPUs
  - Need small (low cost/power/mass) processors for micro-satellites to perform simpler missions
  - Existing use of “radhard” processors does not help with either of these trends
- The microprocessor (main controller) of a spacecraft remains a substantial investment, usually for technology at least one generation old
  - Today: about $50k - $250k for a board based on a processor from the 1990’s or FPGA from early 2000’s
- Usually the processor does not have redundancy, rather being a high reliability radiation hardened element
  - Especially true in small satellites, which have a small budget to start with
- New software is being more accepted for space use; it needs newer processors
  - Autonomy and AI techniques depend on object oriented programming

Objectives

- Use multiple processors to achieve the same performance as modern “radhard” devices
  - Demonstrate the same fault-tolerance performance as ‘radhard” processors
    - Demonstrate that radiation *tolerance* is sufficient when redundancy can overcome any upsets
  - Create redundancy in critical functions while fully utilizing the remainder of the processing capabilitis for other functions
  - Enhance performance by allowing the use of newer COTS microprocessors, and/or
  - Demonstrate sufficient performance from new generation MCU’s to have the same capabilities of “radhard” microprocessors
- Create a cost-effective increase in sub-system redundancy
- Reduce total power requirements
- Utilize the same of smaller board area (m^3 and kg) as a “radhard” system
- Reduce satellite bus manufacturing without reducing performance
  - Achieve the performance using COTS parts at regular industry prices

Architecture Overview

- Utilize multiple interconnected small footprint (cost, mass power) COTS micro processors and/or micro controllers to create a fault-tolerant system with similar performance as a custom “radhard” processor
  - Enable future spacecraft to utilize current generation electronics, rather than depend on the small supply of “radhard” processors
- Utilize “complete system” processors
  - Reduce component count and complexity
  - E.g. PIC, AVR, ARM
- Shared robust bus
  - E.g. CAN bus
- Processors check each other using the bus
- Develop “robust/redundant” I/O
- Towards no single-point failure (for critical tasks)

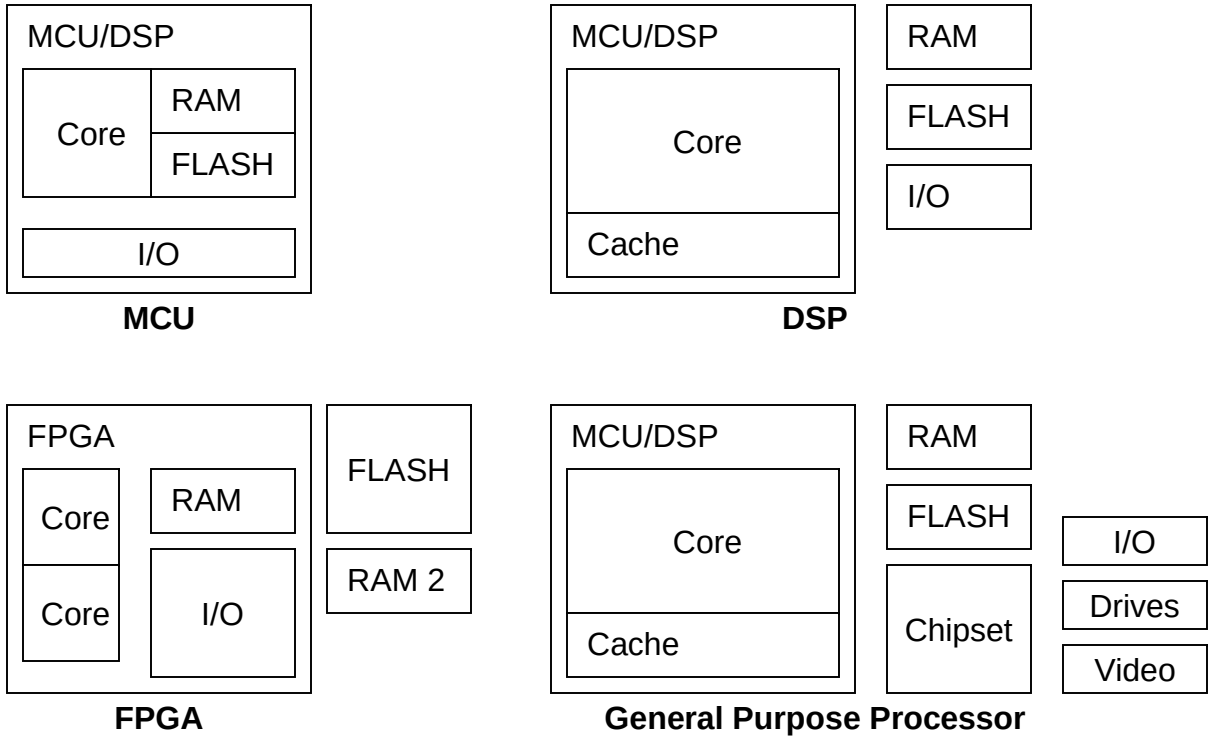


Processor Architectures Review

- Four main architectures compared:
  - MCU - single-chip solutions to very spcific and limited applications. Include processor core, memory, DIO, common communication buses. They do not have strong mathematical functions.
  - DSP - core unit designed specifically for mathematical functions. Low power consumption. Needs external memory and interface IC's to create DIO and communication buses. Highly optimized for mathematical functions, including availability of single-instruction floating point cores. TI C6701 "radhard" version has been used in multiple space missions.
  - General Purpose MP - core unit designed for general applications, not usually used in embedded systems. Needs external memory and interface IC's to create DIO and communication buses. Usually have the highest performance, but require the most development work. The PowerPC has been adopted for space use, with existing "radhard" versions in use.
  - FPGA - it is common to find FPGA's implementing virtual processors, especially PowerPC cores, as part of the "system on a chip" trend. Their implementation in an FPGA sometimes enables them to not need any external components. "Radhard" FPGA's are expected in 2010.

Processor Architectures (2)

- Of the four technologies, MCUs do not need external components. FPGA's require external non-volatile memory. DSP's and general purpose processors require the most external elements.



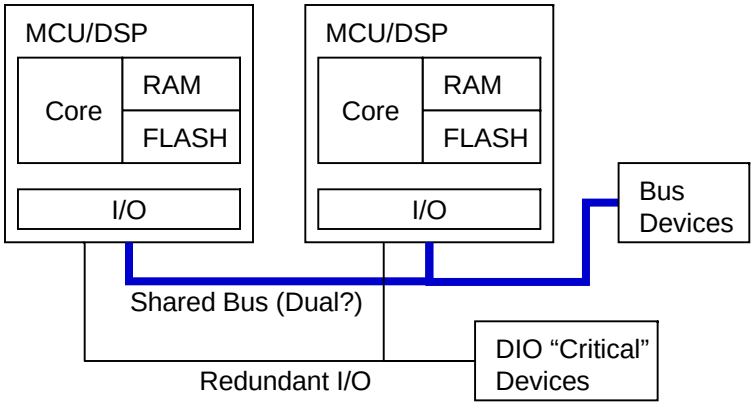
State of the Art Processors

- The table lists some of the newest processors in all four categories
  - General purpose processors provide the most MIPS, but also consume the most power
  - Radhard processors have capabilities like the processors of 10 years ago
  - MCU's have the least capabilities, but only a few of them could be combined to achieve most capabilities of current "radhard" processors

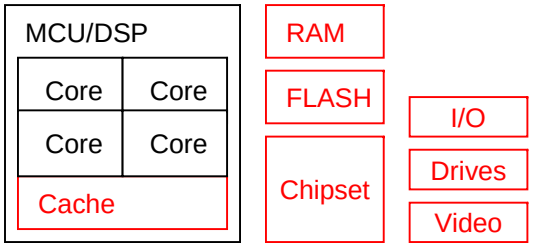
Processor	MHz	MIPS (min/max)	Program Memory	Data Memory	Cache	External Parts	I/O	Power	$
MicroChip MCU PIC32MX360F256L	80	80-124	512k	32k	16	None	Many	0.25W	$8
Atmel MCU AT91SAM9XE512	210	210	512k	32k	24k	Optional	Many	0.33W	$22
C6701DSP (radhard)	140	140-1G	512k - 16MB	16MB-128MB	512k	Multiple	None	2W	>$4000
PowerPC RAD750 (radhard)	132	260	4MB	36MB	1M	Multiple	Bus	25W	>$200k
Intel Core2 Extreme Quad	2500	up to 10,000	4GB+	up to 8GB	12M	Many	Bus	45W	$1200
FPGA: PowerPC NASA MSL	400	600	2G	256MB	TBD	Min 1	Many	2W	$800

Multi Processor Architectures

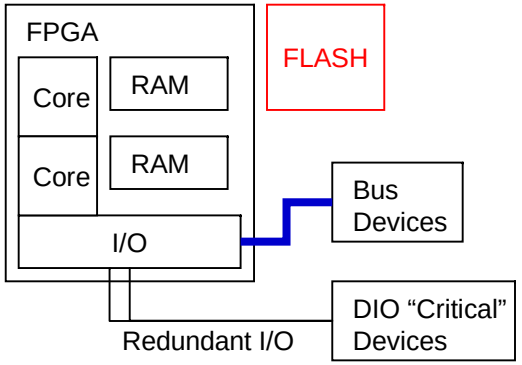
- "Multi-core" products have increased the interest in multi-processor systems
  - We want to use the same algorithms, whiel ensuring that its possible to create a fully redundant system (no single-point failures)
- General purpose multi-core systems have too many shared components
- FPGA designs could be used, as long as multiple FPGA's with multiple external FLASH IC's are used
  - MSL has similar concepts to MultiChipSat, but currently is implementing everything on a single FPGA
    - Robust to SEU's which can be overcome by a system reset
    - Not robust to permanent HW failures (ie, silicon damage)



MultiChipSat MCU's



General Purpose Processor



FPGA (with added redundancy)

Software Architecture

- MultiChipSat involves the development of a *Kernel* which provides oversight of the multi-processor system
- Two main fields in computer science
  - *Parallel processing*: achieving full redundancy of critical tasks and using parallel threads to improve performance of overall system
  - *Voting algorithms / graceful degradation*: enable fault detection and isolation, followed by recovery algorithms that return the processor(s) to a valid state in case of recoverable failures or put the system in a valid reduced capability state where critical tasks still complete
    - *Evolutionary Recovery Electronics* research at JPL detects functionality changes in FPTA's and reconfigures the array to recover the functionality, specifically to address radiation issues in sub 0.5micron process IC's.
      (Adrian Stoica, Tughrul Arslan, et al, "Evolutionary Recovery of Electronic Circuits from Radiation Induced Faults")

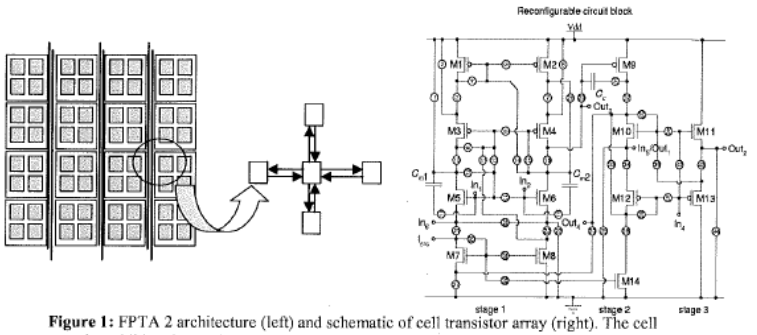


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

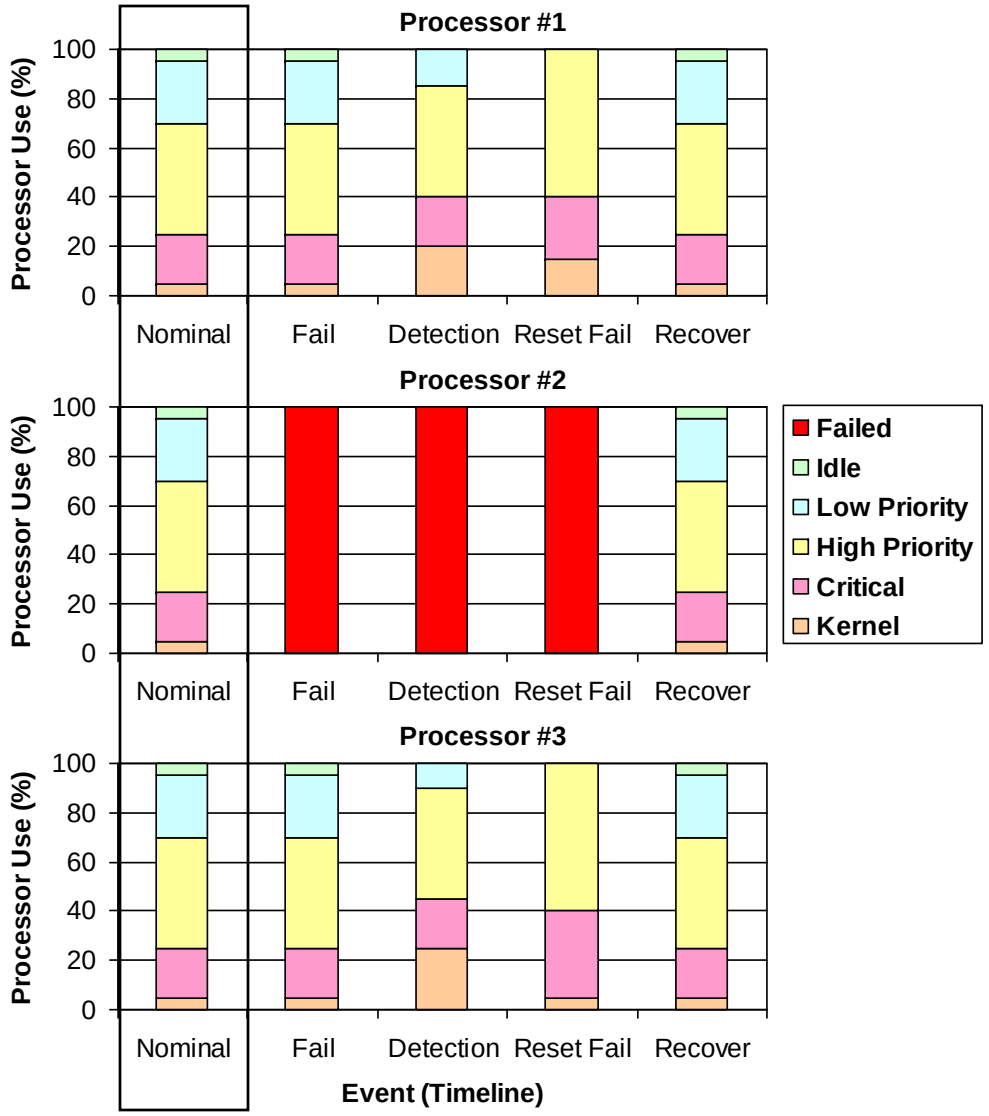
Failure Types

- Single-Event-Upsets
  - data corruption which results in a processor creating a bad output or halting operations
  - the event is recoverable by restarting the processor and returning to a known state
- Permanent Hardware Failures
  - high energy particles physically damage the silicon in the processor, rendering it inoperable
  - the software must then re-distribute the load of critical tasks and stop performing non-critical tasks that are no longer possible

SW Example (1)

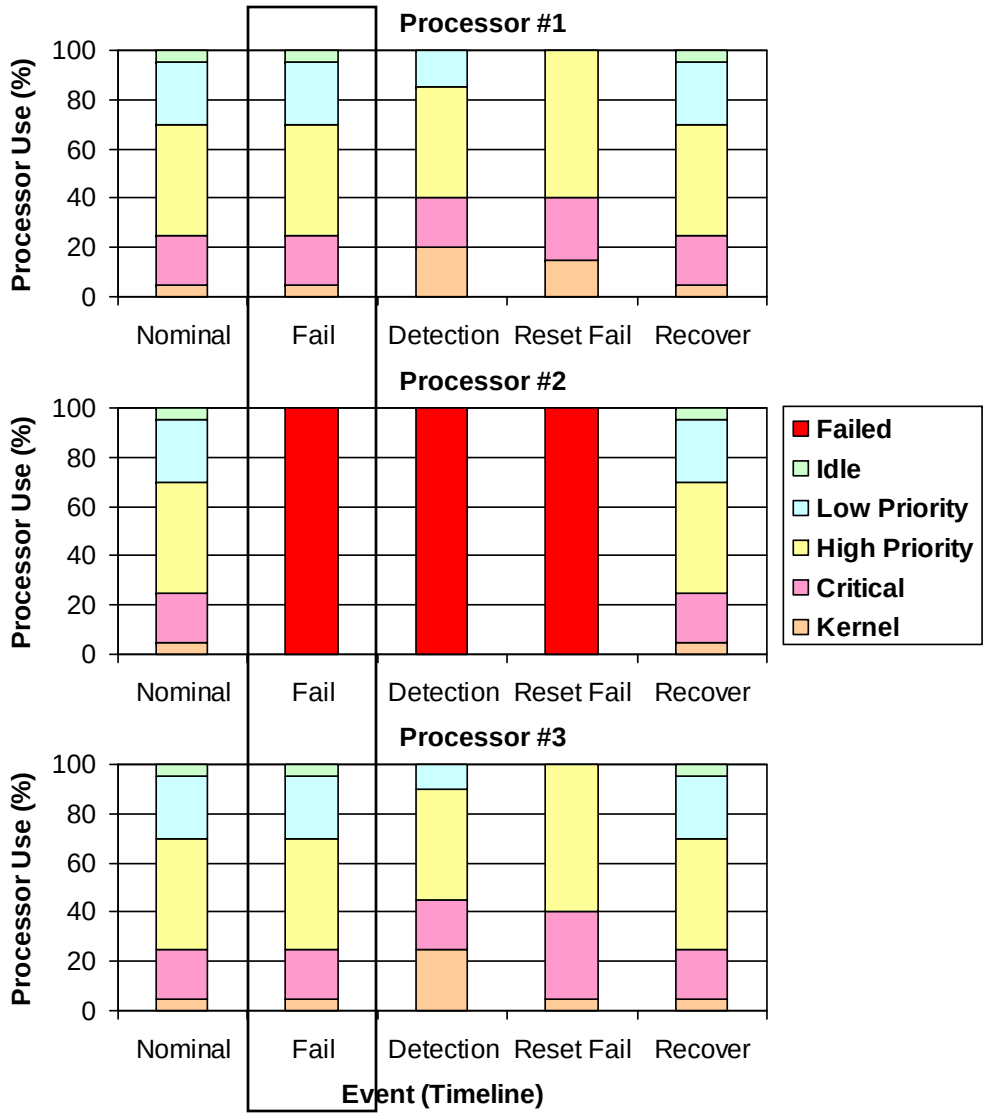
- Kernel: the OS developed for MultiChipSat
- Critical: tasks required to maintain the satellite operational
- High Priority: collecting the necessary data
- Low Priority: processing data locally (reducing comm req)
- Idle: margin

- Nominal operations
  - Kernel has minimal impact
  - All operations complete, including low priority tasks



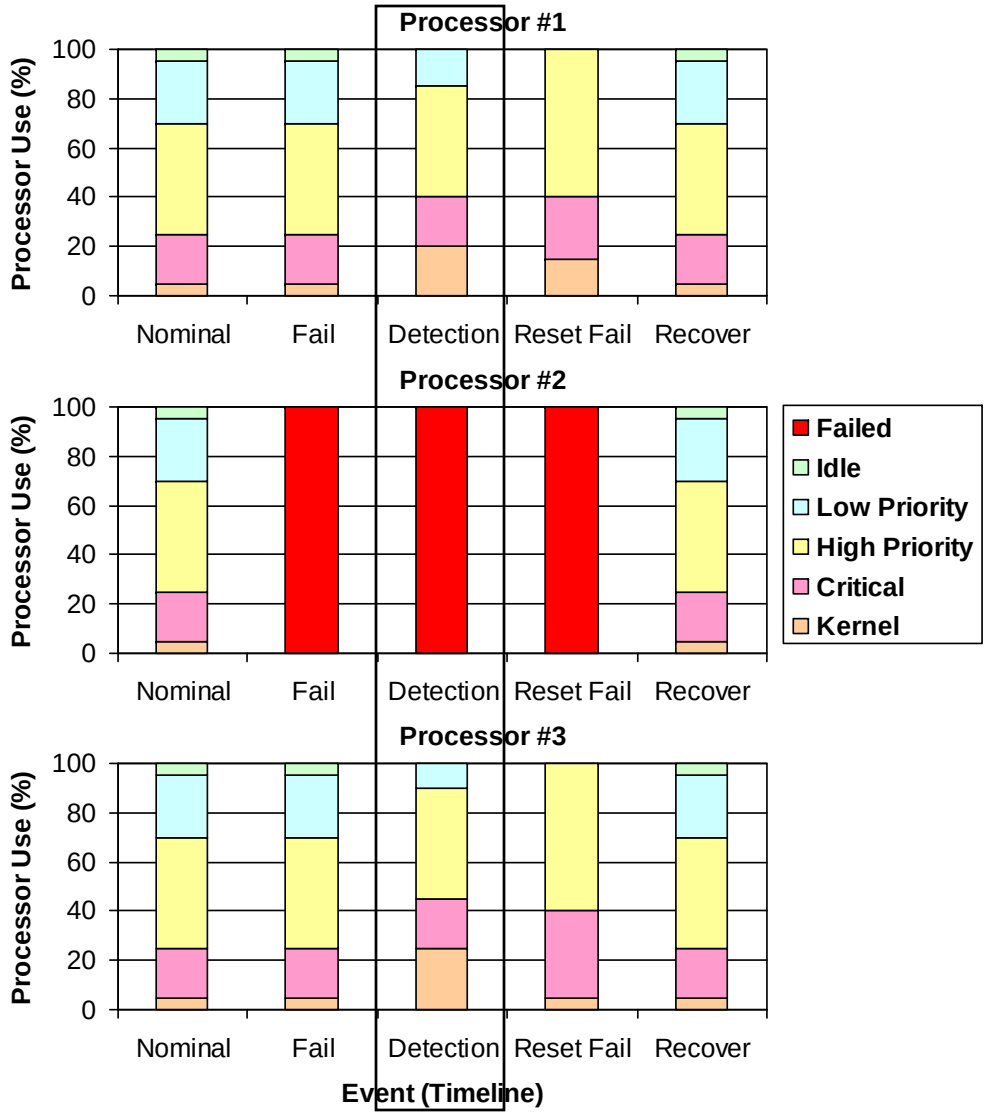
SW Example (2)

- Nominal operations
- Failure occurs
  - One processor stops working completely
  - The other processors initially continue operating as they were, but the kernel is using the shared bus to check for failures...



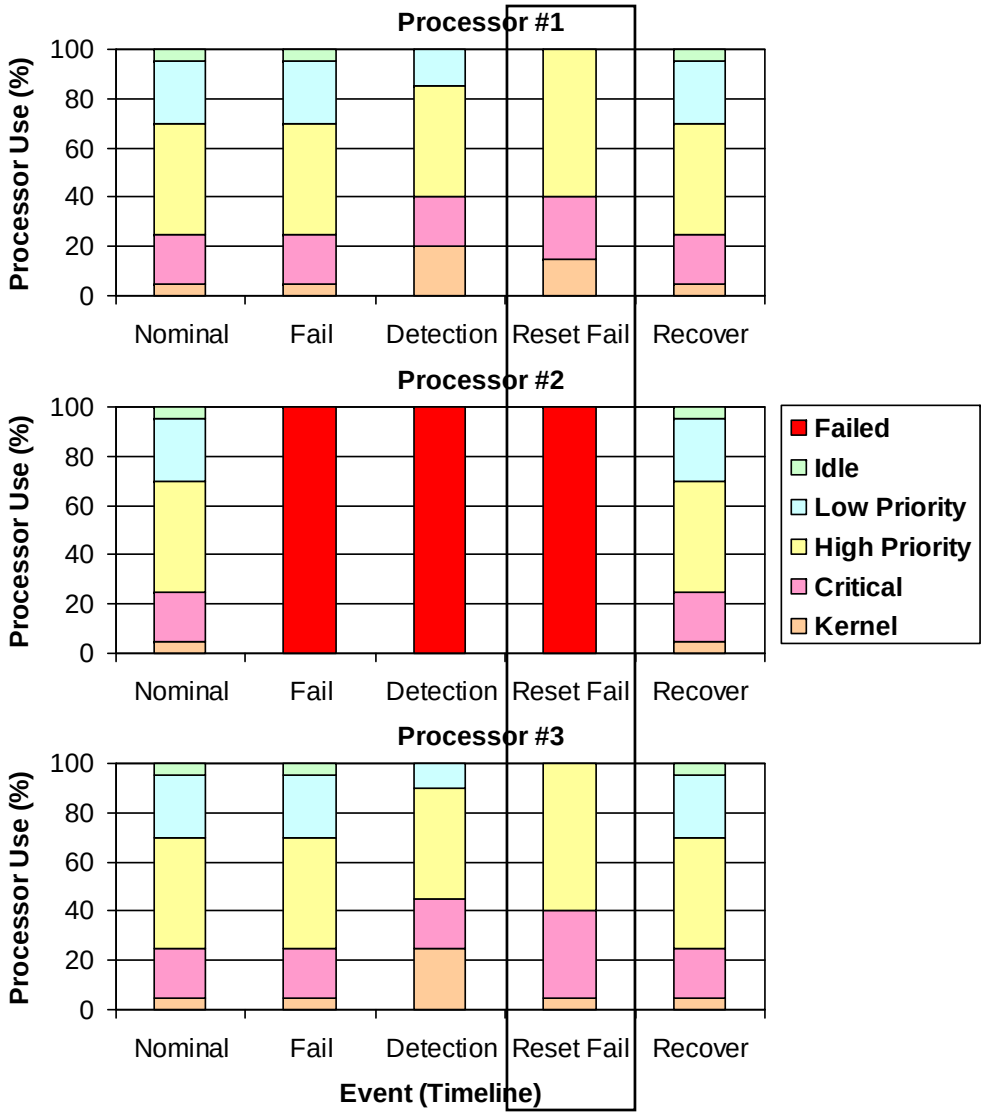
SW Example (3)

- Nominal operations
- Failure occurs
- Error detection
  - The kernel detects a processor has failed
  - Kernel priority increases in operational processors to identify the failure
  - No idle time
  - Low priority tasks may not run



SW Example (4)

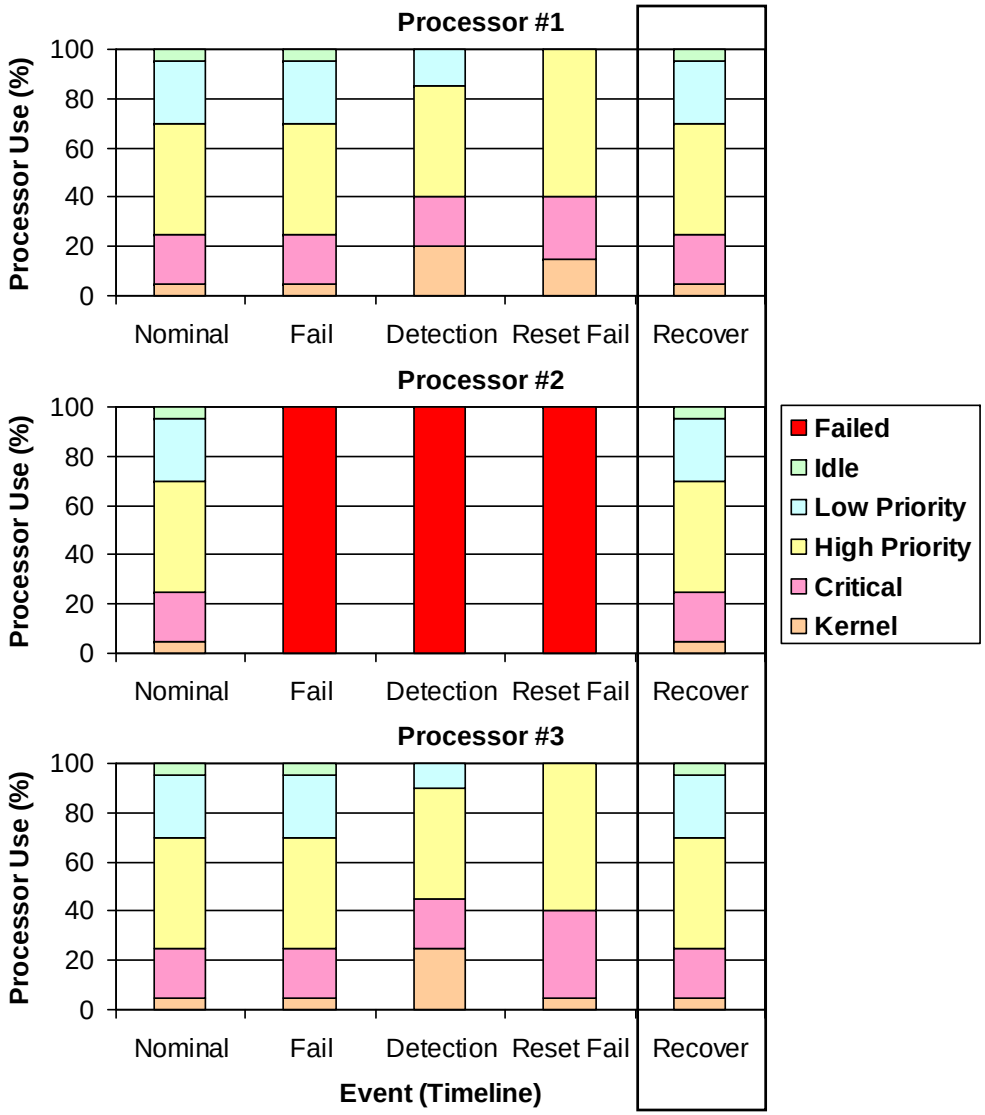
- Nominal operations
- Failure occurs
- Error detection
- Recovery starts
  - The critical & high priority tasks of the failed processor are taken over by the operational processors
    - Low priority tasks are ignored
  - One oversight processor maintains a high priority kernel to find the solution
  - The other processor maximizes its ability to continue critical tasks from the failed processor



SW Example (5)

- Nominal operations
- Failure occurs
- Error detection
- Recovery starts
- Recovery
  - After the failed processor restarts, the oversight processor communicates to it necessary information to return to a valid state for the current operations
  - The processors then return to normal operation

- *Must be able to complete this cycle without negatively affecting satellite operations!*



Main Challenges

- Ensure no single-point failure
  - Both in hardware *and* software - hard to identify single point failures in software
  - Single-point failures in I/O: how to combine I/O's from multiple MCUs with no or minimal external components
- Large memory/processor requirements for Kernel
  - A Kernel is pressumed to be small and have minimal impact on processing requirements
  - The MultiChipSat Kernel might require more memory and than is normally available in MCU's
- Not considering payload requirements
  - At this point the idea is to demonstrate the concept
  - MCU memory limitations especially of concern for complex payloads
- Not considering rest of avionics system
  - Power systems, signal conditioning, etc
- Demonstration of radiation effects
  - It is not trivial to reproduce the space radiation environment
  - Must initially perform tests with simulated failures; are they good enough?

Potential Benefits

- Considering the process to create a complete system board, MultiChipSat technology could:
  - Improve MIPS if able to utilize new generation microprocessors or
  - Provide equal MIPS to radhard processors with substantial less power/cost requirements
  - Introduce redundancy in processor system
  - Reduced cost by several orders of magnitude
  - Reduce power consumption
  - Reduce implementation time

System	# Processors	MIPS	Power [W]	Cost [$]
RAD750	1	260	25	~$200k
C6701 Space	1	140-1G	2	~$50000
Intel Core2 Quad	3	>7.5G	150	~$6000
Virtex II PowerPC	3	1.8G	6W	~$6000
Atmel MCU	3	630	1W	~$1000
PIC MCU	3	240	0.75W	~$1000

Questions & Comments

Thank you